REMARKS

Claims 25-32 are now in the application. As requested by the examiner, attached are replacement drawings which now show the substrate 13 located below insulating layer 3. The specification has been amended at page 7 to reflect the amendment provided by the replacement drawings. The replacement drawings and amendment to the specification do not introduce any new matter.

The objection to the specification as containing new matter and the objection to claims 25 and 31-32 are not deemed tenable. The specification as originally filed explicitly discloses that recesses are formed in at least one major surface of the semiconductor substrate. For instance see page 1, lines 14-16 of the original disclosure that state:

"This is achieved by selectively plating recesses in a semiconductor substrate with conductive metal such as copper or gold."

Also, see original claim 25 as filed which states "recesses located in at least one major surface of said semiconductor substrate." In addition, see the original Abstract of the Disclosure that states:

"Recesses in a semiconductor structure are selectively plated ....."

Accordingly, the above recitation is not new matter and claims 25, 31 and 32 properly recite "in."

Claims 25-32 were rejected under 35 USC 112, first based upon non-enablement in the recitation "a conductive barrier located over said insulation layer in said recess and over said at least one major surface" and a conductive metal in said recesses only."

This rejection is not deemed tenable. In particular, the reference to the "conductive barrier located over said at least one major surface" refers to structure as shown in Figure 7 which illustrates barrier layer 4 located over at least one major surface as well as an intermediate structure that would exist between figures 3 and 4, prior to removal of the barrier layer down to the insulating layer. For instance, see page 12, lines 11-27 of the original disclosure that states:

> "The conductive material 8 can then be chemically–mechanically polished to remove small amounts of metal above the surface of the recesses. Typical polishing slurries contain colloidal silica.
>
> Next, the barrier layer 5 and plated metal is removed down to the insulating layer 3 (see Fig. 4)." (emphasis mine)

Claims 25, 28-29 and 31-32 were rejected under 35 US 102(e) as being anticipated by U.S. Patent 5821168 to Jain.

Jain does not anticipate the above claims, since, among other things, the recesses 72 in insulating layer 52 of Jain do not exist in a semiconductor substrate as recited in the claims. The recesses exist only on the substrate.

Accordingly, Jain fails to anticipate the present invention. In particular, anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. *See Titanium Metals Corp. v. Banner,* 227 UPSQ 773 (Fed. Cir. 1985), *Orthokinetics, Inc. v. Safety Travel chairs, Inc.* 1 UPSQ2d 1081 (Fed. Cir. 1986), and *Akzo N.V. v. U.S. International Trade Commissioner,* 1 USPQ2d 1241 (Fed. Cir. 1986).

There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. 102. *See Scripps Clinic and Research Foundation v. Genetech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to Deposit Account No. 22-0185.

Respectfully submitted,

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